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10/583,518	06/16/2006	Shunsaku Muraoka	071971-0637	1431

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EXAMINER	
LAPPAS, JASON	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/583,518	MURAOKA ET AL.	
	Examiner	Art Unit	
	Jason Lappas	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *06/16/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 8 is objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim should refer to other claims in the alternative only. See MPEP § 608.01(n). Accordingly, the claim has not been further treated on the merits.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 8 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1 to 4 are from a different set of claims than 5 and 8. initialization method therefore is not pointed out.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Liu (U.S. Patent 6,204,139).

Claim 1. Liu discloses a method for initializing a material (variable-resistance material CMR and HTSC taught in Liu abstract) whose resistance value increases/decreases according to the polarity of an applied electric pulse (increase and decrease of resistance depending on polarity of ±12V of electric pulses, Liu Fig 4a), wherein an electric pulse having a first polarity (-12V Fig 4a) is applied at least once between first and second electrodes (application of voltage between first and second electrodes of resistive element is inherent) connected to the variable-resistance material such that the potential of the first electrode is higher than that of the second electrode (since the voltage switches to ±12V, one electrode has to be at a higher potential than the other).

Claim 2. Liu discloses the first electric pulse is repeatedly applied between the first and second electrodes (see the first four electrical pulses at -12V of Fig. 4a, Liu) till the variation rate of the resistance value of the variable-resistance material becomes smaller than a predetermined value (second -12 pulse already shows a smaller variation as it begins to flatten at the peak. First peak has a variation of approximately 15Ω (405Ω-390Ω), second peak variation is significantly smaller variation),

Claim 3. Liu discloses an electric pulse having a second polarity (+12V Fig. 4a) is applied at least once between first and second electrodes connected to the variable-

resistance material such that the potential of the first electrode is lower than that of the second electrode (-12V is less than 6V) ,

Claim 4. Liu discloses the second electric pulse is repeatedly applied between the first and second electrodes (following +12V of Fig. 4a) till the variation rate of the resistance value of the variable-resistance material becomes smaller than a predetermined value (for the last +12V electrical pulses the variation is smaller than the previous which is approx 25Ω (200Ω-175Ω)).

5. Claims 5-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Ignatiev (U.S. Patent 6,473,332).

Claim 5. Ignatiev discloses a memory device (RAM Ignatiev Fig 5) formed using a material (variable-resistance material Rmulti in Fig 5 composed of 208 Fig 2, PCMO or LSMO or GBCO) whose resistance value increases/decreases according to the polarity of an applied electric pulse (CMR, Abstract as well as Col 4 lines 9-13), comprising:
a variable-resistance material (208, Fig 2) to which first (212) and second (214) electrodes are connected; and
a fixed resistor (Rin 520, Fig 2), one end of which is connected to the first or second (one end of Rin is connected to one of the electrodes of 504 through transistors shown in Fig 5) electrode wherein an electric pulse is applied for recording between the first and second electrodes (see Fig. 5 and Fig. 6 as well as Col 10 lines 44-65).

Claim 6. Ignatiev discloses memory information is read based on a voltage (VR, Fig 7) between the first and second electrodes which is obtained when a predetermined voltage (VS) is applied between one of the first and second electrodes which is not connected to the one end of the fixed resistor and the other end of the fixed resistor (the broadest reasonable interpretation of "one and the other" is "both". it is not connected to both ends, just one end of Rin is connected to one of the electrodes of 504 through transistors shown in Fig 5, the other is connected to ground),

Claim 7. Memory information is read based on a voltage (potential of input node of differential amplifier 502, Fig 5) between the ends of the fixed resistor which is obtained when a predetermined voltage (Vs) is applied between one of the first and second electrodes which is not connected to the one end of the fixed resistor and the other end of the fixed resistor (it is not connected to both ends, just one end of Rin is connected to one of the electrodes of 504 through transistors shown in Fig 5, the other is connected to ground).

Claim 8. The variable-resistance material (208, Fig 2) is initialized in advance by the initialization method recited in any one of claims 1 to 4 (initialized by write operation, see Fig. 5 and Fig. 6 as well as Col 10 lines 44-65).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu (U.S. Patent Application Publication 20030003674) in view of Liu (U.S. Patent 6,204,139).

Claim 9-11. Hsu discloses in a memory circuit including first (52, Fig 3 connected to W1 and B1) and second (variable resistor under 52 connected to W1 and B2) variable resistors connected in series between a first terminal (node at B1) and a second terminal (node at B2) wherein

the first variable resistor being connected between the first terminal (node at B1) and a third terminal (node on W1) and having a resistance value which increases/decreases according to the polarity of a pulse voltage applied between the first terminal and the third terminal (Hsu [0028]), and the second variable resistor being connected between the third terminal (node on W1) and the second terminal (node at B2) and having a resistance value which increases/decreases according to the polarity of a pulse voltage applied between the third terminal and the second terminal ([0028]). Hsu also discloses

a block erase method wherein both cells are put at the same time to the same high or low resistance value (see paragraph [0025] and [0027]), therefore, Hsu discloses the steps of applying a first pulse voltage having a first polarity between the first terminal and the third terminal at least once and applying a second pulse voltage having a second polarity between the third terminal and the second terminal at least once. In Hsu the two variable resistors are made of $Gd_{0.7}Ca_{0.3}BaCo_2O_{5+5}$ with bottom electrode made of YBCO or PCMO with bottom electrode made of platinum ([0014] and [0015]). It is noted that Hsu is silent with respect to applying a first pulse voltage having a first polarity between the first terminal and the third terminal at least once and applying a second pulse voltage having a second polarity between the third terminal and the second terminal at least once and applying a third pulse voltage having a polarity opposite to the pulse voltage applied just before to both variable resistors.

Liu Fig 4a teaches when these variable resistors have not yet been subjected to application of a pulse voltage (electrical pulse number 0), they have an arbitrary initial resistance which corresponds neither to their high or low resistance state read afterwards during operation. Liu discloses that by applying a first pulse voltage and after an opposite pulse voltage, the variable resistors are initialized and afterwards achieve stable high or low resistance value.

Since Hsu and Liu are both from the same field of endeavor (applying pulses with opposite polarity), the purpose disclosed by Liu would have been recognized in the pertinent art of Hsu.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to, in an initial state where the first and second resistors have not yet been subjected to application of a pulse voltage, perform a block erase, (apply a first pulse voltage having a first polarity between the first terminal and the third terminal at least once and applying a second pulse voltage having a second polarity between the third terminal and the second terminal at least once), and after this block erase, to apply a third pulse voltage having a polarity opposite to the pulse voltage applied just before to both variable resistors (at least one variable resistor would be programmed) for the purposes of achieving stable high or low resistance values.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Lappas whose telephone number is (571)270-1272. The examiner can normally be reached on M-F 7:30AM-5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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